

ABSTRACT OF THE DISCLOSURE

Delay time between an input of data to a circuit block and an output of the data from the data block is measured in accordance with a timing at which the data from the circuit block is acquired by a measurement register and a timing at which the data from the circuit block is acquired by a data latch. An LSI tester sets well voltage adjustment values so that delay time of each circuit block is averaged. From voltages generated by the adjustment voltage generating circuit, a selector selects voltages that are in accordance with the well voltage adjustment values. The voltages selected are applied to a well of a CMOS transistor of each clock timing adjustment circuit. Delay time between timings of inputted clocks is thus adjusted.